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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/980,754	02/15/2002	Wilfred Lerch	Az. 2964	7497

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/980,754	LERCH ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The addition of claims 51 and 52 as set forth in paper filed on 07/26/2004 is acknowledged.

2. Claims 45 and 47 were not ~~were not~~ included in the rejection mailed on 03/22/2004.

3. A new rejection is included in this Office Action to include a rejection of all of the pending claims.

4. Claims 28-52 are pending in the application.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 28, 31-36, 39, 41-44, 46-49, 50 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilk et al. (U.S. 6,274,510 B1) in view of Thakur et al. (U.S. 6,274,510 B1).

In reference to claims 28, 44, 46, 49 and 50, Wilk et al. (Figs.1a-1d) teach a method of forming a thermally grown silicon nitride gate dielectric layer including forming a 4 nm thick silicon nitride layer (20) directly on the surface of a substrate (10), wherein said substrate contains foreign atoms (column 3, lines 26 – 28), wherein said silicon nitride layer (20) is formed by subjecting said substrate (10) to a thermal treatment protocol comprising a single step process, wherein said substrate (10) was

previously cleaned, wherein said foreign atoms are thermal budget limited, i.e., thermal dependent, and wherein said foreign atoms are doped implant regions; and forming a field effect transistor including source/drain regions (column 3, line 17 – column 4, line 35).

Wilk et al. fail to expressly teach wherein said treatment protocol causes the action of controlling at least one of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere such that the subsequent concentration and diffusion of foreign atoms within said semiconductor material are influenced by the newly created respective concentration or distribution of defects or vacancies in said semiconductor material, wherein the distribution of foreign atoms within the semiconductor material is controlled by means of distribution of said defects. However, the recited results would be obtained because the same materials are treated in the same manner.

Still Wilk et al. fail to teach producing the silicon nitride layer on the surface of the substrate at which a natural silicon dioxide layer has been previously removed prior to the thermal treatment. However, Thakur et al. (Figs.1-8) in a related deposition method teach producing a silicon nitride layer (20) on a semiconductor substrate (10) wherein said substrate (10) is cleaned of a natural silicon dioxide layer prior to the formation of said silicon nitride layer (20) (column 4, line 13 – column 5, line 30). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wilk et al. and Thakur et al. to enable the cleaning step of Wilk et al. to be performed according to the teachings of Thakur et al. because one of ordinary skill in the art at the time the

invention was made would have been motivated to look to alternative suitable methods of performing the disclosed cleaning step of Wilk et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claims 31 – 36, the combined teachings of Wilk et al. and Thakur et al. teach wherein a composition of the process gas is controlled (column 3, lines 42 – 52); wherein a concentration of a process gas or of process gas components is controlled (column 4, lines 24 – 33); wherein a partial pressure of a process gas is controlled (column 3, lines 53 – 56); wherein a process gas includes a nitrogen-containing gas (column 3, lines 42 – 52); wherein said process gas includes at least NH_3 (column 3, lines 42 – 52); and wherein a process gas contains no oxygen (column 3, lines 42 – 52).

In reference to claim 39, the combined teachings of Wilk et al. and Thakur et al. teach wherein a temperature behavior is controlled in terms of time (Thakur et al., column 2, lines 60 – 65).

In reference to claims 41 and 42, the combined teachings of Wilk et al. and Thakur et al. substantially teach all aspects of the invention but fail to disclose wherein said process includes NH_3 at a concentration of 0 to 10,000ppm, and wherein said NH_3 has a concentration from 2,500 to 5,000ppm. However, the selection of the claimed ranges is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. Therefore, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to use the above-mentioned range to arrive at the claimed invention.

In reference to claim 43, the combined teachings of Wilk et al. and Thakur et al. substantially teach all aspects of the invention but fail to disclose wherein the process reduces thermal stressing of the semiconductor substrate. However, the same material would be treated in the same manner and therefore the recited results would be obtained.

7. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilk et al. ('510 B1) in view of Thakur et al. ('510 B1) as applied to claims 28, 31-36, 39, 41-44, 46, 49 and 50 above, and further in view of the Applicants Admitted Prior Art.

The combined teachings of Wilk et al. and Thakur et al. substantially teach all aspects of the invention but fail to expressly teach wherein said defects are vacancies or interstitial lattice positions, and wherein said foreign atoms include boron atoms. However, the prior art teaches that the implantation of boron atoms on a substrate and its subsequent thermal treatments enable the formation of defects, and wherein said foreign atoms include boron atoms (instant page 1, line 13 – page 2, line 17). Furthermore, the submitted disclosure states that said defects are either vacancies or interstitial lattice positions (page 17, lines 18 – 20). Therefore, the combined teachings of Wilk et al. and Thakur et al. inherently teach the above-mentioned limitation.

8. Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilk et al. ('510 B1) in view of Thakur et al. ('510 B1) as applied to claims 28, 31-

36, 39, 41-44, 46, 49 and 50 above, and further in view of Aronowitz et al. (U.S. 6,087,229).

The combined teachings of Wilk et al. and Thakur et al. teach wherein the substrate is doped (column 3, lines 17 – 40). The combined teachings of Wilk et al. and Thakur et al. fail to disclose wherein a process gas includes an oxygen-containing component; and wherein said oxygen-containing component includes at least one of N_2O, NO, and H_2O. However, Aronowitz et al. (Figs.2-4) in a related method to prevent diffusion of foreign atoms from a substrate (202) that is to be doped, to devices fabricated on it, teach subjecting the substrate (202) to a thermal process to form a silicon nitride layer (206); and subjecting said substrate (202) to a subsequent thermal treatment, producing a silicon oxynitride layer (206) by subjecting said substrate (202) to a process gas comprising steam (column 6, line 51 – column 8, line 16). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wilk et al. and Thakur et al. with the teachings of Aronowitz et al. to enable the deposition step of Wilk et al. and Thakur et al. to be performed according to the teachings of Aronowitz et al. because one of ordinary skill in the art at the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed deposition step of Wilk et al. and Thakur et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

9. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilk et al. ('510 B1) in view of Thakur et al. ('510 B1) as applied to claims 28, 31-36, 39, 41-44, 46, 49 and 50 above, and further in view of Gardner et al. (U.S. 6,218,720 B1).

The combined teachings of Wilk et al. and Thakur et al. substantially teach wherein the process gas comprises ammonia and nitrogen (Thakur et al., column 6, lines 11 – 15). The combined teachings of Wilk et al. and Thakur et al. fail to teach wherein the process gas contains argon. However, Gardner et al. (Fig.7) teach forming a nitride layer (210) on the surface of a substrate (200) by subjecting the substrate to a thermal treatment in a nitrogen-containing atmosphere, wherein the process gas used comprises either ammonia and nitrogen, or ammonia and argon (column 8, lines 14 – 34). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the process gas of Wilk et al. and Thakur et al. according to the teachings of Gardner, since this would provide the further advantage of providing control of the formation of the nitride layer on the silicon surface by slowing the nitridation process (column 8, lines 14 – 27).

10. Claims 45 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilk et al. (U.S. 6,274,510 B1) in view of Thakur et al. (U.S. 6,274,510 B1) and Wolf et al. (Silicon Processing for the VLSI Era, Volume 1: Process Technology).

Wilk et al. (Figs.1a-1d) teach a method of forming a thermally grown silicon nitride gate dielectric layer including forming a 4 nm thick silicon nitride layer (20) directly on the surface of a substrate (10), wherein said substrate contains foreign atoms (column 3, lines 26 – 28), wherein said silicon nitride layer (20) is formed by

subjecting said substrate (10) to a thermal treatment protocol comprising a single step process, wherein said substrate (10) was previously cleaned, wherein said foreign atoms are thermal budget limited, i.e., thermal dependent, and wherein said foreign atoms are doped implant regions; and forming a field effect transistor including source/drain regions (column 3, line 17 – column 4, line 35).

Wilk et al. fail to expressly teach wherein said treatment protocol causes the action of controlling at least one of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere such that the subsequent concentration and diffusion of foreign atoms within said semiconductor material are influenced by the newly created respective concentration or distribution of defects or vacancies in said semiconductor material, wherein the distribution of foreign atoms within the semiconductor material is controlled by means of distribution of said defects. However, the recited results would be obtained because the same materials are treated in the same manner.

Still Wilk et al. fail to teach producing the silicon nitride layer on the surface of the substrate at which a natural silicon dioxide layer has been previously removed prior to the thermal treatment. However, Thakur et al. (Figs.1-8) in a related deposition method teach producing a silicon nitride layer (20) on a semiconductor substrate (10) wherein said substrate (10) is cleaned of a natural silicon dioxide layer prior to the formation of said silicon nitride layer (20) (column 4, line 13 – column 5, line 30). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wilk et al. and Thakur et al. to enable the cleaning step of Wilk et al. to be performed according to

the teachings of Thakur et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed cleaning step of Wilk et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Wilk et al. and Thakur et al. fail to teach wherein said foreign atoms include at least one of the elements of the group consisting of boron, phosphorous, As, Sb, and In. However, Wolf et al. teach conventional gaseous dopants (i.e., foreign atoms) used in the fabrication of diffused regions in semiconductor wafers include boron, phosphorous, As and Sb, wherein said diffusion processes are thermally controlled (page 264-265). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Wilk et al. and Thakur et al. with the teachings of Wolf et al. to enable forming the diffused regions of Wilk et al. and Thakur et al. using the foreign atoms disclosed in Wolf et al., because these are common materials used in the formation of diffused regions in the preparation of semiconductor wafers (Wolf et al., page 264).

Response to Arguments

11. Applicant's arguments filed 07/26/2004 have been fully considered but they are not persuasive.

Applicants argue, "...it can be seen that Wilk et al. '510 provides no teaching nor suggestion concerning such a two-step treatment protocol in which the preliminary step includes controlling at least one of a concentration and a distribution of defects or

vacancies as a function of a process gas atmosphere such that the subsequent concentration and diffusion of foreign atoms within the semiconductor material are influenced by the newly created respective concentration or distribution of defects or vacancies in the semiconductor material...". In response to this argument, Wilk et al., teach forming a thermal nitride and controlling the thermal budget of diffused region in the semiconductor substrate during the formation of said nitride layer. Taking this into consideration, Brigham et al. to U.S. 5,714,413 teach a method forming a silicon nitride layer, wherein the temperature used for the formation of said nitride affects the distribution of diffused regions within the semiconductor substrate (column 3, lines 30 – 48 and column 5, lines 52 – 67). Since Wilk et al. teach using the same materials the same way the same result would be expected. Therefore, Wilk et al. teach upon that limitation.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
October 15, 2004

George Fourson
Primary Examiner